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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,910	03/26/2004	Manabu Ohnishi	60188-823	7704

7590 07/20/2005

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/809,910	OHNISHI ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☒ Claim(s) *10-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/26/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 03/26/2004 is acceptable.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1 and 3-7** are rejected under 35 U.S.C. 102(e) as being anticipated by Ali et al. U.S. Patent 6,836,026 (the '026 reference).

The '026 reference discloses in Figures 5 and 7 and respective portions of the specification a semiconductor device as claimed.

Referring to **claim 1**, the reference discloses a semiconductor device formed by flip-chip bonding a semiconductor chip to a carrier used for external connection with the semiconductor chip (column 5, last full paragraph for the limitation flip-chip bonding; see Wu et al. U.S. Patent Application Publication 20030230792, paragraph [0003], for a description how a flip-chip chip must be bump-bonded to a carrier), wherein:

the semiconductor chip (56, Fig. 5; Fig. 7) includes:

a plurality of input/output cells (52, Fig. 5; 66,70, Fig. 7) including circuit elements formed so as to be peripherally arranged on a surface of the semiconductor chip, and

a plurality of electrode pads (42; 72,74) formed on associated ones of the input/output cells ("on" is interpreted broadly, see Figs. 5 and 7 of the '026 reference and Fig. 2 of the present invention;

the electrode pads are configured in a zigzag pad arrangement so as to form inner and outer pad arrays (as evident in Fig. 5, and as indicated to be "modifiable" in Fig. 7, column 10, lines 50-58); and

a predetermined area (58, or 58 and electrode pads near a corner and adjacent to region 58; the area in Fig. 7 that is right at a chip's corner that is nearest to the I/O cell 62 or 68 that is right at the corner) near a corner on the semiconductor chip surface is designated as a pad-disposition restriction area (58), within which disposing and usage of one or ones of the electrode pads that are bump-bonded to an interconnect pattern formed on a surface of the carrier are restricted.

Referring to **claim 3**, although not explicitly disclosed, the extent of the pad-disposition restriction area (58) is determined in accordance with design rules for the carrier.

Referring to **claim 4**, the reference further discloses that in the pad-disposition restriction area, part of the inner pad array is not formed.

Referring to **claim 5**, the reference further discloses that in the pad-disposition restriction area, a pitch for the outer pad array is reduced in accordance with minimum separation rules regarding disposition of the input/output cells (column 5, last full paragraph).

Referring to **claim 6**, the reference further discloses that in the pad-disposition restriction area, neither the inner pad array nor the outer pad array is formed.

Referring to **claim 7**, the reference further discloses that in the pad-disposition restriction area (58), instead of some of the input/output cells which correspond to the inner and outer pad arrays, other types of function cells (core logic 58, column 8, lines 25-30) are disposed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claim 2** is rejected under 35 U.S.C. §103(a) as being unpatentable over Ali et al. U.S. Patent 6,836,026 (the '026 reference).as applied to claim 1 above, and further in view of Tokuno JP02000164620A (cited by Applicant).

The '026 reference discloses a semiconductor device as claimed and as detailed above including the electrode pads 42, but fails to teach that the each of the electrode pads has a tenon-like conformation in plan view, and includes a narrow, probing portion for testing or analyzing, and a wide, bonding portion which is bump-bonded to the interconnect pattern on the carrier surface.

Tokuno, in also disclosing a semiconductor device including electrode pads, teaches that electrodes such arranged allows for inspection and bonding to be performed easily and surely, in addition to a lessened influence of the probe marks.

Therefore, it would have been obvious to form the reference's device such that each of the electrode pads has a tenon-like conformation in plan view, and includes a narrow, probing portion for testing or analyzing, and a wide, bonding portion which is bump-bonded to the interconnect pattern on the carrier surface. One would have been motivated to make such a change in view of the teachings in Tokuno that such change allows for inspection and bonding to be performed easily and surely, in addition to a lessened influence of the probe marks.

4. **Claims 8-9** are rejected under 35 U.S.C. §103(a) as being unpatentable over Ali et al. U.S. Patent 6,836,026 (the '026 reference).as applied to claim 1 above, and further in view of Pappert et al. U.S. Patent 5,929,650 or in view of Phillips et al. U.S. Patent 5,671,234, or vice sersa.

The '026 reference discloses a semiconductor device as claimed and as detailed above including the inner pad array and the pad-disposition restriction area, but fails to teach that in the pad-disposition restriction area, the inner pad array includes probing-specific pads for testing or analyzing, and is not bump-bonded to the interconnect pattern on the carrier surface.

Pappert, in disclosing a semiconductor device , teaches that (pads at) corners of a chip are unavailable for bond out due to thermal and mechanical stresses, which often result in passivation cracking and other reliability issues, and that the use of these expendable portions (the corners) of the die allows for efficient testing that does not impinge on the functionality or available circuit area of the device (column 3, lines 34-49).

Therefore, it would have been obvious to form the reference's device such that in the pad-disposition restriction area (the corners), the pad array, inner and outer, includes probing-

carrier surface. One would have been motivated to make such a change in view of the teachings in Pappert that such change allows for the utilization of the otherwise useless space of the chips.

As for the limitation of **claim 9**, it is within the ability of a person of ordinary skill in the art at the time the invention was made to chose, as required, such that, in the pad-disposition restriction area, only one or ones of the electrode pads of the inner pad array are individually bump-bonded to the interconnect pattern on the carrier surface, therefore, such ability to chose would have been obvious.

Phillips, in disclosing a semiconductor device , teaches that test pads in one corner of the integrated circuit die permits easy probing of the integrated circuit (column 16, lines 32-41).

Therefore, it would have been obvious to form the reference's device such that in the pad-disposition restriction area (the corners), the pad array, inner and outer, includes probing-specific pads for testing or analyzing, and is not bump-bonded to the interconnect pattern on the carrier surface. One would have been motivated to make such a change in view of the teachings in Phillips that test pads in one corner of the integrated circuit die permits easy probing of the integrated circuit.

Alternatively, Phillips discloses in Fig. 9 all limitations as claimed in claim 8 including probing-specific pads 301 for testing or analyzing and not for being bump-bonded to the interconnect pattern on a carrier surface, but fails to teaches that the electrode pads are configured in a zigzag pad arrangement so as to form inner and outer pad arrays. The '026 reference, as detailed above for other claims, teaches that arraging electrode pads in a zigzag pad arrangement so as to form inner and outer pad arrays allows for more bonding pads to be formed (column 6, lines 38-42). Therefore, it would have been obvious to form Phillips' device such

that the electrode pads are configured in a zigzag pad arrangement so as to form inner and outer pad arrays. One would have been motivated to make such a change in view of the teachings in the '026 reference that such zigzag pad arrangement allows for more bonding pads to be formed.

Allowable Subject Matter

5. Claim 10 and dependent claims 11-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a semiconductor device formed by flip-chip bonding a semiconductor chip to a carrier used for external connection with the semiconductor chip having all limitations of claim 10, characterized in that in the pad-disposition restriction area, the inner pad array is individually bump-bonded to the interconnect pattern on the carrier surface, and at least two of the electrode pads are short-circuited to each other inside the carrier.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
July 12, 2005